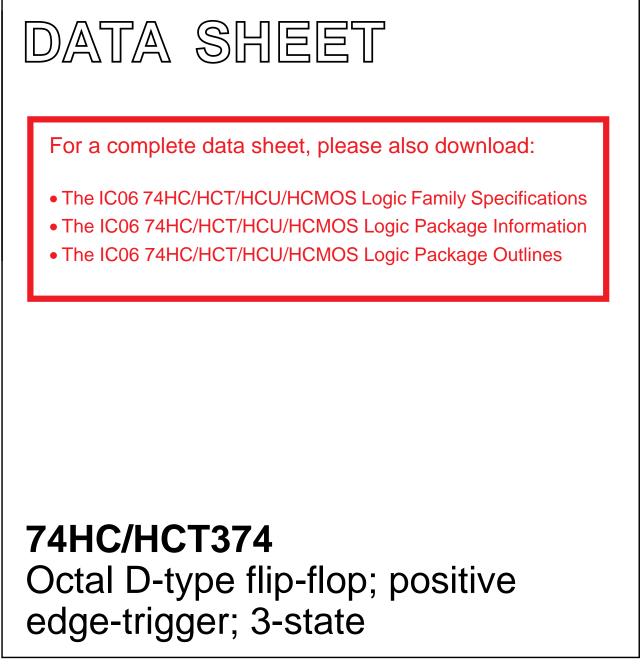
INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC06 December 1990



74HC/HCT374

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

 $GND = 0 \text{ V}; \text{ } T_{amb} = 25 \text{ }^{\circ}C; \text{ } t_r = t_f = 6 \text{ } ns$

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable (\overline{OE}) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When \overline{OE} is LOW, the contents of the 8 flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYP			
STWIDOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
t _{PHL} / t _{PLH}	propagation delay CP to Q _n	$C_{L} = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	15	13	ns	
f _{max}	maximum clock frequency		77	48	MHz	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF	

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz

 f_0 = output frequency in MHz

 $\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

 C_{L} = output load capacitance in pF

 V_{CC} = supply voltage in V

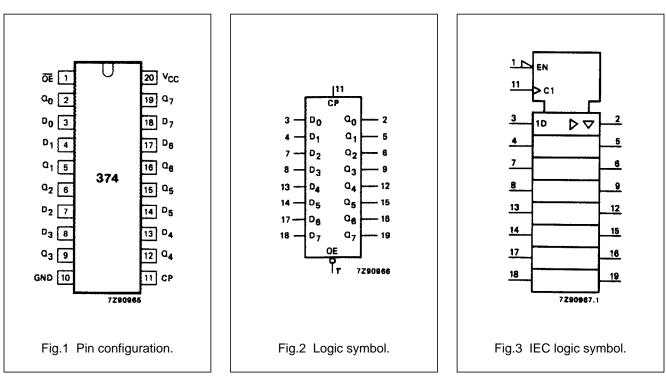
2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

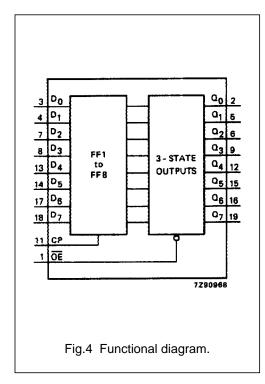
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	СР	clock input (LOW-to-HIGH, edge-triggered)
20	V _{CC}	positive supply voltage



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FUNCTION TABLE

OPERATING		NPUT	S	INTERNAL	OUTPUTS		
MODES	ŌE	СР	D _n	FLIP-FLOPS	Q ₀ to Q ₇		
load and read register	L	↑ ↑	l h	L H	L H		
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z		

Notes

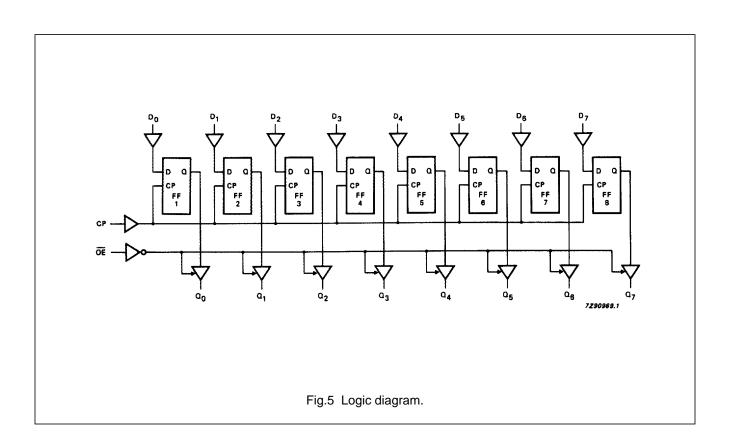
1. H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

- Z = high impedance OFF-state
- \uparrow = LOW-to-HIGH CP transition



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C)								TEST CONDITIONS	
SYMBOL	PARAMETER	74HC									WAVEFORMS
		+25			-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig.6
t _{PZH} / t _{PZL}	$\frac{3\text{-state output enable time}}{\overline{OE}} \text{ to } Q_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{PHZ} / t _{PLZ}	$\frac{3\text{-state output disable time}}{\overline{\text{OE}} \text{ to } Q_n}$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t _W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t _{su}	set-up time D _n to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t _h	hold time D _n to CP	5 5 5	-6 -2 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
f _{max}	maximum clock pulse frequency	6.0 30 35	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
ŌĒ	1.25
CP	0.90
D _n	0.35

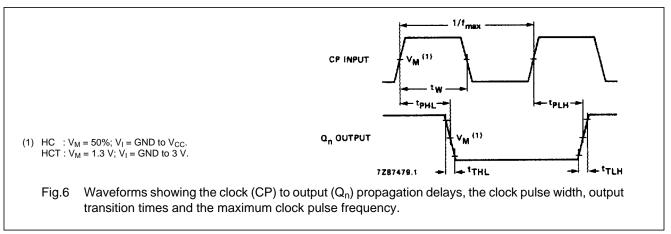
AC CHARACTERISTICS FOR 74HCT

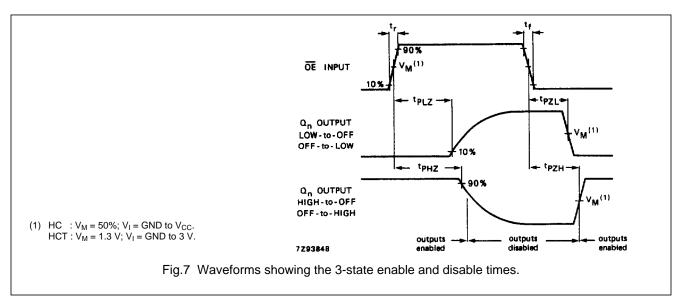
 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

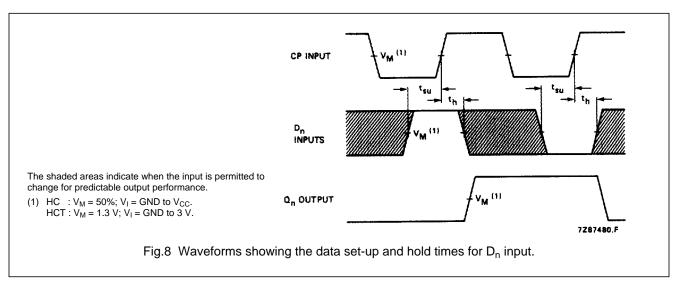
SYMBOL		T _{amb} (°C)								TEST CONDITIONS		
	PARAMETER	74HCT									WAVEFORMO	
		+25			-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(•)		
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		16	32		40		48	ns	4.5	Fig.6	
t _{PZH} / t _{PZL}	$\begin{array}{c} 3\text{-state output enable time} \\ \overline{\text{OE}} \text{ to } Q_n \end{array}$		16	30		38		45	ns	4.5	Fig.7	
t _{PHZ} / t _{PLZ}	$\begin{array}{c} \text{3-state output disable time} \\ \overline{\text{OE}} \text{ to } Q_n \end{array}$		18	28		35		42	ns	4.5	Fig.7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6	
t _W	clock pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig.6	
t _{su}	set-up time D _n to CP	12	7		15		18		ns	4.5	Fig.8	
t _h	hold time D _n to CP	5	-3		5		5		ns	4.5	Fig.8	
f _{max}	maximum clock pulse frequency	26	44		21		17		MHz	4.5	Fig.6	

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AC WAVEFORMS







PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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